L7: Entry 5 of 9 File: USPT Apr 8, 1997

DOCUMENT-IDENTIFIER: US 5619726 A
** See image for Certificate of Correction **
TITLE: Apparatus and method for performing arbitration and data transfer over multiple buses

Detailed Description Text (24):
Upon receiving a C1-bus Request from the external peripheral device or the Arbiter/DMA element 220, the C1-bus arbitration element 275 transmits a HOLD signal to the microcontroller through a first C1-bus control line 276 in an attempt to gain access to the C1-bus. At an appropriate time, the microcontroller transmits a Hold Acknowledge ("HLDA") signal to the Arbiter/DMA element 220 through a second C1-bus control line 277 signaling that the microcontroller has relinquished control of the C1-bus. Thereafter, the C1-bus arbitration element 275 arbitrates HLDA between the C1-bus masters, providing such access to the C1-bus master having the highest priority. If the HOLD signal is based on a C1-bus request by the Arbiter/DMA element 220, the C1-bus arbitration element 275 forwards the arbitrated HLDA signal ("AHLDA signal") to the Arbiter/DMA element 220 via a third C1-bus control line 278.

CLAIMS:

1. An apparatus coupled between a first bus and a second bus, said apparatus comprising:

arbitration means for arbitrating ownership of the first bus for a plurality of first bus masters and for arbitrating ownership of the second bus for a plurality of second bus masters, said arbitration means including a first arbitration element, a second arbitration element and at least one programmable storage means for providing programmable access priorities for each of said plurality of second bus masters to said second arbitration element, said second arbitration element awarding ownership of the second bus based on said access priorities; and

DMA transfer means for performing a DMA transfer between a first component coupled to the first bus and a second component coupled to the second bus when the apparatus has simultaneous ownership of both the first and second buses, said DMA transfer means being coupled to said arbitration means.

24. A computer system comprising:

a plurality of first bus masters including a first component, said first component including at least one of processor means for processing information and first storage means for storing said information;

first bus means for coupling together said plurality of first bus masters;

a plurality of second bus masters including a second component, said second component including at least one of auxiliary processor means for processing information and second storage means for storing said information processed by said at auxiliary processor means and for storing application-related information;

second bus means for coupling together said plurality of second bus masters; and

arbiter/DMA means for arbitrating ownership of said first and second bus means and performing a DMA transfer between said first bus means and said second bus means, said arbiter/DMA means including:

arbitration means for arbitrating ownership of the first bus for said plurality of first bus masters and for arbitrating ownership of the second bus for said plurality of second bus masters, said arbitration means, coupled to said plurality of first bus masters and said plurality of second bus masters, and

DMA transfer means, coupled to said arbitration means, for performing a DMA transfer between the first component and the second component when the arbiter/DMA means has simultaneous ownership of both the first and second bus means.

27. A computer system comprising:

a first plurality of bus masters including a first component;

first bus means for coupling together at least said first plurality of bus masters;

a second plurality of bus masters including a second component;

second bus means for coupling together at least said second plurality of bus masters; and

arbiter/DMA means for arbitrating ownership of said first and second bus means and performing a DMA transfer between said first bus means and said second bus means, said arbiter/DMA means including:

arbitration means for arbitrating ownership of the first bus means and for arbitrating ownership of the second bus means, said arbitration means, coupled to said first plurality of bus masters and said plurality of second bus masters, including a plurality of arbitration elements and at least one programmable storage means for providing programmable access priorities for each of said plurality of second bus masters to said second arbitration element, and

DMA transfer means, coupled to said arbitration means, for performing a DMA transfer between the first component and the second component when the arbiter/DMA means has simultaneous ownership of both the first and second bus means.